THE ALCATEL 9343 DVB-OBP PRODUCT: AN ON-BOARD PROCESSOR FOR DIGITAL TELEVISION AND INTERNET DATA

Y. Le Roy (1), J. Prat (1) & A. Jalón (1)
J. Riba (2), J. Sala (2) & I. Morrison (3)

(1) ALCATEL ESPACIO (AEO)
C/ Einstein, 7 - 28760 Tres Cantos (Spain)
Email: yves.roy@space.alcatel.es

(2) Universitat Politècnica de Catalunya (UPC)
Department of Signal Theory and Communications
Campus Nord, Ed. D-5, Jordi Girona 1, 3 - 08034 Barcelona (Spain)
Email: jriba@gps.tsc.upc.es

(3) Turbo-Communications Ltd (TCL)
16, West Barnes Lanes - London SW20 OBU (England)
Email: ian@turbocomms.co.uk

INTRODUCTION

The Alcatel 9343 DVB-OBP (On-Board Processor) payload is aimed at providing broadcast of digital multi-program television and Internet to the European countries. AEO, UPC and TCL have developed the payload under ESA contract within the DOMINO-2 program. The basic concept is to provide access to individual broadcasters and service providers. A single carrier conveying all programs received on individual up-links based on the Digital Video Broadcasting - Return Channel Satellite (DVB-RCS) standard, and fully compliant with the Digital Video Broadcasting by Satellite (DVB-S) standard, is transmitted on the down link. Provision is also made for on-board cross-connection facilities between DVB-forward transponders.

This paper presents a brief overview of the DVB system and a detailed description of the processor architecture referred to as Base Band Processor (BBP). Each unit of the product is described in terms of performances and functionality and the final paragraph gives an overview of the budgets.

SYSTEM DESCRIPTION

The A9343 ALCATEL system integrates a Broadcasting Multi-Media network with an Interaction network into one unique regenerative and multi-spot satellite system. In this system, the DVB-RCS return channel standard is applied to all users for accessing through a standard uplink to the satellite. On board, the regenerative payload is in charge of multiplexing that information from diverse sources into one or more DVB-S data streams capable of being received by standard IRD equipment.

The A9343 system is based on a fully regenerative On-Board Processor designed to provide direct (distributed) DVB-RCS (EN-301-790) compliant satellite access for individual digital video broadcasters, Internet Service Providers, and multimedia users. Individual users and broadcasters can access the satellite on any of several uplink coverage footprints illuminated by the satellite, using multiple frequencies, within a TDMA frame, and at several transmission rates. The satellite downlink completely satisfies the DVB-S Standard (EN-300-421) in order to take advantage of the economies of scale and the performance of standard commercial DVB-S IRDs. Fig. 1 illustrates the concept.

The system up-link of a given transponder is characterised by an access of multi-carriers of transmission rates of Rs, 2Rs, 4Rs, 8Rs and 16 Rs (Rs = 0.3278 M symb/s).
The uplink parameters of the A9343 are the following (the parameters which vary with the rates are included in table 1):

- Framing: MPEG-2 Transport Stream
- Coding Turbo-Code: (DVB-RCS 6/7, 4/5)
- Energy dispersal: according to DVB-RCS
- Modulation: QPSK, roll-off 0.35
- Access: MF-TDMA
- Carrier spacing: 1.5 k.Rs (k = 1, 2, 4, 8 and 16)
- Information data rates: k.Ri (Ri = 0.518 Mbps and k = 1, 2, 4, 8 and 16)

<table>
<thead>
<tr>
<th></th>
<th>k=1</th>
<th>k=2</th>
<th>k=4</th>
<th>k=8</th>
<th>K=16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Information Rate</td>
<td>0.5184 Mbit/s</td>
<td>1.0368 Mbit/s</td>
<td>2.0735 Mbit/s</td>
<td>4.1471 Mbit/s</td>
<td>8.2941 Mbit/s</td>
</tr>
<tr>
<td>Transmission Rate</td>
<td>0.3278 Msymb/s</td>
<td>0.6557 Msymb/s</td>
<td>1.3114 Msymb/s</td>
<td>2.6227 Msymb/s</td>
<td>5.2454 Msymb/s</td>
</tr>
<tr>
<td>Traffic Burst in one frame</td>
<td>1,2,4,6,18</td>
<td>1,2,4,6,18</td>
<td>1,2,4,6,18</td>
<td>1,2,4,6,18</td>
<td>1,2,4,6,18</td>
</tr>
<tr>
<td>Packets per Burst</td>
<td>24,12,6,4,1</td>
<td>24,12,6,4,1</td>
<td>24,12,6,4,1</td>
<td>24,12,6,4</td>
<td>24,12,6,4,1</td>
</tr>
<tr>
<td>Number of carriers</td>
<td>up to 72</td>
<td>up to 36</td>
<td>up to 18</td>
<td>up to 9</td>
<td>up to 4</td>
</tr>
</tbody>
</table>

Table 1: Data rates and number of users in TDMA mode for code rate 6/7

The frequency plan divides a transponder of 36 MHz into 5 sub-bands (see frequency plan in demultiplexer section), 4 of which have a capacity of 16 Rs and one has a capacity of 8 Rs. Each sub-bandwidth can be configured independently as 16/k carriers of k.Rs (k = 1, 2, 4, 8 and 16) for the 16Rs sub-bandwidths and 8/k carriers of k.Rs (k = 1, 2, 4, 8 and 8) for the 8Rs sub-bandwidth. The system reference clock is 27 MHz and is located on board. This clock is used by the broadcasters to synchronise the symbol rate of the uplink bursts. The synchronisation process is carried out according to the DVB-RCS standard.
The downlink is a DVB-S standard flow including the required coding and modulation. The output transmission data rate is 54 Mbps derived on the reference on-board clock of 27 MHz. The number of Rs carriers which can be inserted in the downlink flow depends on the rate of the convolutional code and is detailed in table 2.

<table>
<thead>
<tr>
<th>CVR=1/2</th>
<th>CVR=2/3</th>
<th>CVR=3/4</th>
<th>CVR=5/6</th>
<th>CVR=7/8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Rs Channels</td>
<td>48</td>
<td>64</td>
<td>72</td>
<td>80</td>
</tr>
</tbody>
</table>

Table 2: Number of Rs channels in downlink flow

**BBP EQUIPMENT DESCRIPTION**

A general diagram of the BBP is presented in figure 2 and the equipment consists of two main parts:

- the OBP module which includes all the specific parts of the On-Board Processing
- the Control and Supply module which consists of the DC/DC, TM/TC and clock modules

The OBP module consists of the following boards:

- MC3D board which includes 6 ASICs (1 DEMUX ASIC and 5 DEMDEC ASICs) to carry out the following functions:
  - Analogue to Digital Conversion (ADC)
  - Demultiplexing (DEMUX) of carriers included in a 36-MHz bandwidth in order to generate elementary carriers of kRs (k=1, 2, 4, 8, 16) in 4 sub-bands of 16Rs and carriers of k’Rs (k=1, 2, 4, 8) in one sub-band of 8Rs
  - Parallel demodulation (DEMDEC) of 16/k carriers of rate kRs
  - Turbo decoding of MPEG-2 packets (DEMDEC) generated from the 16/k carriers in order to obtain quasi error-free data (BER < 10^{-10})
  - Storage of output packets in buffers (DEMDEC) in order to have them ready to be requested by the switch or the multiplexer

- Switch board: expands the interfaces of the multiplexers from 8 to 20 by means of an ASIC (SWITCH ASIC); this board includes a nominal and a redundant SWITCH ASIC and is implemented if the number of transponders is greater than 6

- Mux board: carries out the functions of packet multiplexing and DVB coding by means of I and Q channels in base-band; 3 ASICs (MUX ASIC) are implemented in this board and are in charge of generating the DVB multiplex for 3 transponders.

The Control and Supply module consists of the following boards:

- Clock board: this board generates all the required clocks for the processing of the DVB as well as the frame synchronisation signal (Start Of Frame); the 78.6 MHz clock is used for the receive chain (ADC, Demultiplexing, demodulation) and the 54 MHz clock is used from the packet decoder to the generation of the DVB flow.

- TM/TC board: is in charge of the control and monitoring of the boards of the BBP with the other modules of the satellite. This function is implemented by a FPGA.

- Power Distribution Module board: converts the regulated voltage (100 V) of the primary bus into secondary voltages for the different units. This board is basically composed of 4 DC/DC blocks which provide the secondary voltages to the other boards

The Control and Supply module have been redunred in order to avoid single point failures and cold redundancy is applied between the two modules. The three elements of a module work in a solidar form in such a way that, when the DC/DC board is supplied, the Clock board and the TM/TC boards of the same module are also supplied. Cold
redundancy has also been implemented between the 2 SWITCH ASICs and any ASIC can be supplied with the nominal or redundant systems for the clocks and the supply voltages (no TM/TC bus for this ASIC).

Fig. 2 : Decomposition of BBP into boards

If the number of transponders is lower than or equal to 6, all the boards are integrated in a single box. In case that this number is greater than 6, for reasons of power module dimensioning and interface design, it is planned to separate the Base Band Processor into 2 kinds of equipments (see figure 3) and to include the Switch board in the design: the first class of equipment shall include the MC3D boards (MC3D equipment) and the second class shall include the switch boards, the mux boards and the clock boards (Switch-Mux-Coding or SMUCO equipment). Each class of equipment shall include its own DC/DC and TM/TC boards and the clocks shall be transmitted from the SMUCO box to the MC3D boxes as shown in the figure. A maximum number of 20 transponders with full cross-connection can be managed by the separated equipments. As an indication, 3 MC3D boxes will be necessary to implement 20 transponders and 2 MC3D boxes can accomodate up to 16 transponders. In any case, a single SMUCO box is necessary and the number of mux boards which are mounted (up to 7) depend on the number of transponders.

Fig. 3 : Decomposition of BBP into several boxes
BBP FUNCTIONALITIES AND PERFORMANCES

The basic functionality of the Base-Band processor consists in obtaining a DVB-S compliant multiplexed stream from filtered IF inputs by means of a receive chain and a multiplexer. In the first part, the receive chain will be described by highlighting the demultiplexer, the demodulator and the decoder and the EbN0 figures required at the input of the chain will be presented. In the second part, the main system functions of the multiplexer will be detailed.

Demultiplexer

The demultiplexing stage is capable of processing a 36-MHz transponder including a multiplex of carriers of five different rates defined as k*Rs, k=1,2,4,8,16. The frequency plan (figure 4) which has been selected consists in splitting the transponder bandwidth into five sub-bands (four sub-bands of capacity 16 Rs and one of capacity 8 Rs). A sampling frequency of 240 Rs (78.68 MHz) has been considered which allows to reserve a 6Rs sub-band (equivalent to 4 Rs carriers with 1.5 Rs spacing) on each side of the multiplex for SAW filtering. A 16-Rs sub-band includes 16/k carriers of kRs and an 8-Rs sub-band includes 8/k (k’=1, 2, 4, 8) carriers of k’Rs. As these sub-bands are represented by physical interfaces, the samples of the demultiplexed carriers are multiplexed in time if several carriers are demultiplexed and there exists the possibility of rotating the sub-bands w.r.t. to the DEMDEC ASICs in order to privilege sub-bands in case of ASIC failure.

5 filtering stages are implemented by means of polyphase filters to perform the demultiplexing into elemental carriers. An Automatic Gain Correction loop is implemented between the first stage and the second stage in order to compensate the level of signal and noise due to the gain variation of the on-board RF and IF receive chains. The measurements are performed on noise only during the silence period of the bursts.

Demodulator

The demodulator is implemented in the DEMDEC ASIC and is in charge of processing the carriers of a sub-band, i.e. 16/k carriers of kRs with k=1, 2, 4, 8, 16. When several carriers are present in the sub-band, the samples are multiplexed in time with a rate of 3 samples per symbol at the input.

The burst structure consists of a preamble of 256 symbols of which 32 are dedicated to a Unique Word followed by useful data. The acquisition/demodulation of a burst consists of the following processing stages:

- Matched filtering which optimises the Nyquist filtering with a roll-off factor of 0.35
- Timing correction which allows to get the optimum sampling moment and to convert the rate of 3 samples/symbol to 1 sample/symbol
- Phase/frequency correction consisting of 4 Kalman algorithms working in parallel

Decoder

The turbo decoder which is implemented in the BBP is fully compliant with the DVB-RCS standard. It is based on the Maximum-A-Posteriori (MAP) principle which gives the best performances but, as its complexity is too elevated to be implemented with space technology, it has been replaced by a Max-Log-MAP algorithm. This algorithm brings a degradation of about 0.2 – 0.5 dB with respect to the MAP algorithm. On the other hand, a 4-bit quantisation scheme for the soft decision input symbols, which brings a degradation of 0.2 dB w.r.t. no quantisation at all, has been selected.
The decoder architecture (see figure 14) works on a packet by packet basis and performs 5 iterations per packet. The input symbol frequency is 16Rs, that is to say 5.25 MHz, and the processing speed is 54 MHz. The following elements are part of the architecture:

An input memory: this buffer is organised in 2 blocks, the first to store an incoming packet (data + redundancy) with its soft decision symbols and the second one to allow the decoder to access the packet which is being processed; this buffer works in ping-pong mode, that is to say the memory areas are interchanged each time a new packet is processed. If the data packet contains N couples (N=752 for MPEG-2 packets), the storage capacity is 2 x N x 4 x 752 x 1/r bits, r being the coding rate.

A SISO engine that works on a sub-iteration basis (natural or interleaved order): it decodes the input packet by using the Max-Log-MAP algorithm and produces extrinsic information memory which will be combined with the input data for the next sub-iteration.

An extrinsic information memory: this buffer stores the quaternary extrinsic information which is computed for each couple in the trellis and which is passed from the current sub-iteration to the next one. If the data packet contains N couples, the storage capacity for this information is 3 x N x q bits, q being the width of an extrinsic information word. When computing the next sub-iteration, this information is combined with the input symbol values in the SISO engine.

An Interleaver / deinterleaver: as the same SISO engine is used alternatively for packets in natural and interleaved order, an interleaving stage is applied to the input packet and extrinsic data and a “deinterleaving” stage is applied to the output extrinsic data in order to store them in natural order.

An output memory to convert the output byte speed from 54/4 MHz to 54/8 MHz

**Fig. 5**: Turbo decoder diagram

**EbN0 budgets for receive chain**

The EbN0 required at the input of the BBP (see table 6) to obtain a quasi-error free performance (BER < 10\(^{-10}\)) is directly related to the EbN0 required at the input of the decoder and the losses generated by the demultiplexer (the lower the carrier rate, the higher the losses due to the number of filtering stages) and the demodulator.

<table>
<thead>
<tr>
<th>Carrier rate</th>
<th>Code rate : 4/5</th>
<th>Code rate : 6/7</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 Rs</td>
<td>6.17 dB</td>
<td>7.17 dB</td>
</tr>
<tr>
<td>8 Rs</td>
<td>6.28 dB</td>
<td>7.28 dB</td>
</tr>
<tr>
<td>4 Rs</td>
<td>6.36 dB</td>
<td>7.36 dB</td>
</tr>
<tr>
<td>2 Rs</td>
<td>6.44 dB</td>
<td>7.44 dB</td>
</tr>
<tr>
<td>1 Rs</td>
<td>6.52 dB</td>
<td>7.52 dB</td>
</tr>
</tbody>
</table>

**Table 3**: Required EbN0 at the BBP input
The purpose of this ASIC is to multiplex packets coming from different sources and to code them in order to generate a data flow at 54 Mbps compliant with the DVB-S standard. The functions which will be highlighted here consist of the management of the multiplex table, the Return Information Memory (RIM) and the Network Clock Reference (NCR) packet generation.

The multiplex table is a 2D array (figure 5) which is scanned on a frame basis by the multiplexer and contains columns of 24 packet corresponding to the number of packets per frame of an Rs carrier. The number of columns depends on the convolutional rate which is used for the data output: it varies from 48 (CVR=1/2) to 84 (CVR=7/8). The content of the multiplex table cells indicate the packet location in terms of:

- Packet source: External source (Mux interface number 1 to 8), RIM or internal packet generation (NCR packets, stuffing packets)
- MC3D number (1 to 20 if switch included)
- Sub-band number (1 to 5)
- Carrier number (1 to 16)
- Flags for optional functions (PCR correction, Multicast, RIM enable)

If a packet from an external source is to be multiplexed, the content of every cell is turned into a serial request signal which is identified by the buffer of the related carrier within the MC3D and this buffer responds by sending a packet to the multiplexer. The requests of all the multiplexer ASICs are emitted in fixed time-slots in order to avoid conflicts (overlapping between request reception and packet transmission) at MC3D level. The multiplex table also takes into account the multicast functionality, which enables to send the same packet from a MC3D board to several multiplexers in the same time slot.

### Multiplex Table Scheme

The Return Information Memory (RIM) functionality allows to exchange specific packets such as signalling or partial table packets between multiplexers. An inter-RIM bus has been designed to route the packets from one multiplexer to another (or to all the multiplexers) by means of a Token bus protocol. The transferred packets are sent to the inter-RIM bus nibble by nibble at a speed of 54/4 MHz which allows a maximum transfer capacity of 54 Mbps on this bus. The multiplexer bus interface is bi-directional (figure 6) and the direction is controlled by the multiplexer depending upon it is receiving or transmitting. A multiplexer ASIC can absorb an average amount of traffic from the inter-RIM bus by assigning the corresponding number of cells as needed to the RIM as a packet source. Input and output buffers of 8 packets have been implemented in the multiplexer in order to absorb peak traffic rates.

### Table:

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>96*cvr</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>96*cvr+1</td>
<td>96*cvr+2</td>
<td>96*cvr+1</td>
</tr>
<tr>
<td>2</td>
<td>96*cvr+2</td>
<td>96*cvr+4</td>
<td>96*cvr+3</td>
</tr>
<tr>
<td>3</td>
<td>96*cvr+4</td>
<td>96*cvr+6</td>
<td>96*cvr+5</td>
</tr>
</tbody>
</table>

Fig. 6 : Multiplex table scheme
The Network Clock Reference (NCR) is a data field included in the MPEG2-TS format that gives continuous count of a 27 MHz clock, divided in a 33 bit base (according to 1/300 division of the 27 MHz clock) and a 9 bit extension (according to the 27 MHz). The inclusion of this reference in dedicated packets (NCR packets) allows the OBP to avoid the initial clock synchronization protocol. This protocol is mandatory for all the units (NCC, broadcast ground stations...), except for the On-Board system which includes this Master Clock. Furthermore, the NCR presence in the downlink is assured independently from any interruption in the uplink normal reception.

**BUDGETS**

The mass and power budgets per transponder are given in figures 8 and 9. It can be seen that the general trend is a decrease of the budgets with the number of channels. However, the fact of incrementing the number of boxes gives way to a rise of weight and consumption, the worst case being the transition from 6 to 7 channels which correspond to the jump from one single box to 2 boxes.

**CONCLUSION**

As shown in the previous sections, the Alcatel-9343 On-Board Processor proves to be a very efficient regenerative subsystem both in terms of receive performances and system functionalities. Maximum EbN0 figures of 6.5 dB (r=4/5) and 7.5 dB (r=6/7) are required at the input to comply with the quasi-error free condition. On the other hand, functionalities such as the routing of specific packets between multiplexers, the multicast feature and the NCR packet generation make this product very attractive for the future generations of on-board regenerative systems.